Performance Evaluation of the High Frame Rate Detector XSPA

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Abstract

In recent years, Hybrid Photon Counting (HPC) detectors have been widely used in the field of X-ray measurement. These detectors display no readout noise and provide a large dynamic range, high frame rate, small point spread function and no blurring. By combining these advantages of HPC detectors with high-speed data readout systems, it is possible to realize a high-performance X-ray detection system with single-photon detection and high detection efficiency. One of the most important elements of HPC detectors is their high-speed readout technology. With the latest HPC detector systems, frame rates of about 1000 fps can be easily realized, which is 1–2 orders of magnitude faster than the frame rate of CCDs, which have been mainstream until now. To meet these demands, the X-ray Seamless Pixel Array (XSPA) detector series was developed. XPSA technology is capable of continuous measurements at 56,000 fps and, with the XSPA Burst Mode, it is possible to achieve intermittent measurements at 970,000 fps. The shortest exposure time for a single frame is 48 nanoseconds. This is achieved by the high-performance UFXC32k chip jointly developed with AGH University and a data readout system that can handle high data rates in real time. In this report, we evaluated the basic performance of the XSPA detector.

1. Introduction

The application of Hybrid Photon Counting (HPC) detectors to X-ray measurements dates back more than 30 years. Many modern X-ray measurement methods are difficult to realize without HPC detectors. For example, X-ray Photon Correlation Spectroscopy (XPCS) and pump-probe measurements, which are advanced tools for observing dynamics, require a detector with a very high frame rate for short time scales. In order to leverage the results of our collaboration with AGH University with respect to the UFXC32k readout IC[(1)], we began to design an HPC detector that can be used for high-frame-rate experiments. In 2014[(2)], we began testing our prototype detectors at various synchrotron facilities worldwide. To achieve a high-frame-rate detector, we have promoted the acceleration of the front-end and back-end readout circuitry and software. As a result of this effort, we have realized an HPC detector capable of continuous measurement at 56,000 fps. With the first detector (Fig. 1), the XSPA-500k (X-ray Seamless Pixel Array), we conducted a series of performance evaluation experiments at the Advanced Photon Source (APS), SPRing-8, Aichi-SR and SOLEIL in collaboration with beamline researchers, AGH University, and Rigaku[(3), (4)].

2. XSPA detector

XSPA detectors, including the XSPA-500k, are HPC detectors with 512k (1024 × 512) of 76 µm × 76 µm sized pixels per module measuring 77.8 mm × 38.9 mm. Sixteen Application Specific Integrated Circuits (ASIC) are tiled on the back side of the monolithic sensor. The UFXC-32k ASIC is described in detail in the following section. The sensor and ASICs are connected on a flip-chip using indium bumps in the same manner as other HPC detectors on the market. However, the XSPA detector is significantly different from other HPC detectors. It has identically sized pixels in the entire area of the sensor. The pixels are 76 µm × 76 µm. In conventional HPC detectors with a total detection area greater than 25 mm × 25 mm, it is common to have inter-chip pixels to avoid contact between neighboring tiled readout ASICs. These inter-chip pixels are 1.5 to 3 times larger on one side and 1.5 to 9 times larger than ordinary pixels in terms of effective area[(5), (6)]. Because these inter-chip pixels correct charges from larger area the information of the hit position is inaccurate compared to ordinary pixels. The counters of the larger pixels saturate more quickly due to their higher count rate so the pixels lose statistical reliability. Conventionally, for experiments that require high statistical precision, we had to mask out these inter-chip pixels so the data would

Fig. 1. XSPA-500k detector.

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not suffer from reduced statistical reliability. To avoid this inter-chip-related inconsistency, we employed a newly developed sensor design in the XSPA detectors[7]. This new design allows all pixels to be handled equally; that is, all pixels have the same performance, which means that the entire detector area can be used for analysis. The standard model of an XSPA detector is equipped with a 320 µm thick Si sensor, which can be replaced with sensors of different thicknesses and composition: Si, GaAs, CdTe, CZT, etc., regardless of the polarity of the collected charge.

2.1. UFXC32k readout chip

UFXC32k (UltraFast X-ray Chip with 32k channels) is an ASIC with a size of 9.64 mm × 20.15 mm and with approximately 50 million transistors using 130 nm CMOS technology[1]. The main part of this integrated circuit is a matrix of 128 × 256, 75 µm × 75 µm sized pixels [Fig. 2(a)]. Each pixel consists of a Krummenacher feedback (feed Krum) Charge-Sensitive Amplifier (CSA), a shaping amplifier (SH) with a minimum peaking time of 40 ns, a threshold setting block (TH), two discriminators (DISCR) and two 14-bit counters (COUNTER) [Fig. 2(b)]. By appropriately setting the current of the feedback discharge block of the CSA, it is possible to tune the tradeoff between the time constant and the noise level suitable for the application[8].

The discriminator threshold is set to a common value, shared by all readout channels, depending on the X-ray energy of interest and the application. The energy threshold is determined by the baseline level and the discriminator threshold. The same value can be set for all pixels, or we can set different values for each pixel. Each pixel has an independent trimming DAC at the input of the two discriminators to minimize the error of the set energy threshold level. Each pixel has the ability to have an independently adjusted gain of the analog front end. In addition, the analog front end can handle both positive and negative (hole and electron) input charges. In combination with excellent leakage current compensation circuitry, the UFXC32k chip can support not only Si but also various sensor materials such as CdTe and GaAs.

When reading data, the counter of each pixel column operates as a shift register, which is written bitwise to a 128-bit high-speed register on the periphery; then, eight parallel Low Voltage Differential Signal (LVDS) lines output the data. The data readout from the chip supports multiple modes, including:

(i) Normal mode, in which each counter operates as two independent 14-bit counters connected to the DISCR-L and DISCR-H.

(ii) A long counter mode, in which two 14-bit counters are combined and connected to DISCR-L as a single 28-bit counter.

(iii) Zero Dead Time (ZDT) mode, in which two 14-bit counters are alternately connected to the DISCR-L. One 14-bit counter performs a read operation as a shift register while the other 14-bit counter is counting, which avoids the occurrence of a temporal gap between frames, and the frame rate can be further improved by reducing the read bit length to a minimum of 2-bit, and continuous operation at a maximum of 56,0000 fps is realized.

(iv) Burst mode, which allows users to shift each counter by 1, 2, or 3-bit for each exposure and obtain data for 23, 11, or 7 exposures at high speed. With the 250 MHz bus clock, the maximum frame rate of 970,000 fps can be achieved.

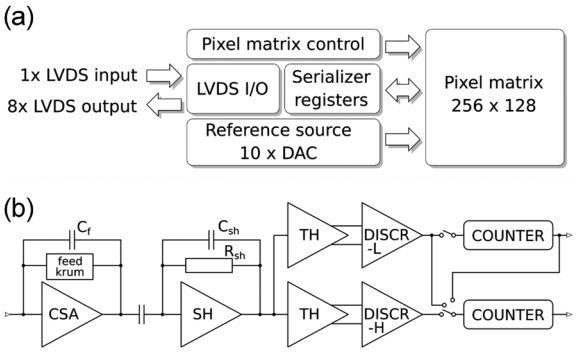

Fig. 2. Schematic configuration diagram of a UFXC32k chip (a) and schematic circuit diagram of a pixel (b).

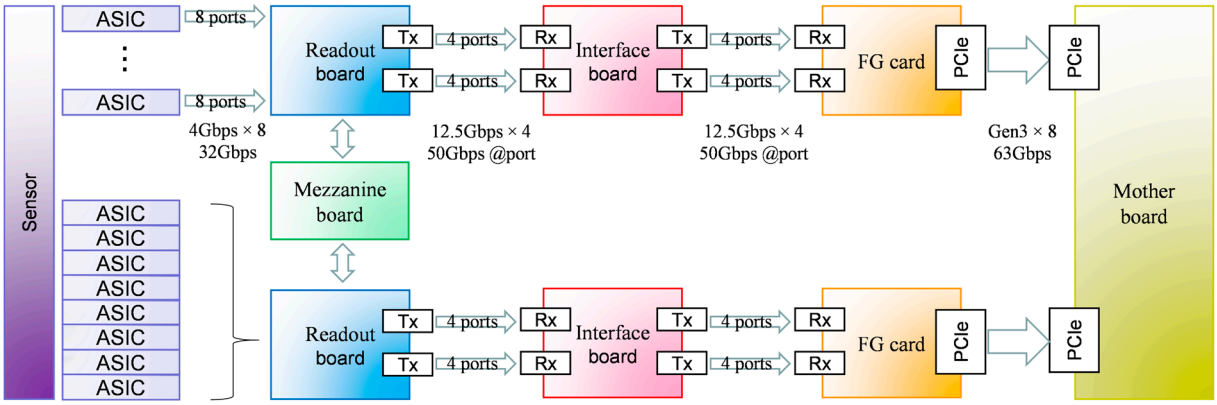

Fig. 3. Schematic diagram of an XSPA detector module (XSPA-500k equivalent).

2.2. Frame Rate

In the front end of the detector, eight ASICs are connected to each of the two readout boards (Fig. 3). The data from each ASIC is sent to the FPGA with a 250 MHz bus clock Double-Data-Rate (DDR). Therefore, the transfer rate from each ASIC is 4 Gbps. Half a module, 8 ASICs, transfers 32 Gbits of data per second to the FPGA. Data transfer from readout boards to the Frame Grabber (FG) cards are done by 8b/10b encoding, 16-bit/pixel (14-bit counter) for a half module. Data of 524,288 bytes becomes 629,146 bytes of traffic; 2-bit/ pixel data of 65,536 bytes becomes 78,644 bytes of traffic. The data transfer rate of each transmitter is 12.5 Gbps and a data port consists of 4 data transmitters, which gives a 50 Gbps maximum data transfer rate. The practical transfer rate is approximately 2/3 of the maximum transfer rate, but the measured bandwidth of PCIe is about 30 Gbps (the theoretical maximum bandwidth is 63 Gbps). This bandwidth limits the readout speed up to 8,500 fps when measured in ZDT mode 16-bit/pixel (14-bit counter), 1,7000 fps for 8-bit/pixel, 33,000 fps for 4-bit/pixel, and 56,000 fps for 2-bit/pixel. Using burst mode, it was possible to read up to 11 frames at 2-bit/pixel and up to 23 frames at 1-bit/pixel at a maximum of 970,000 fps.

3. Detector Performance Evaluation

The XSPA detector was developed by Rigaku and tested with lab sources at Spring-8 (BL26B2, BL29XU), Aichi SR (BL2S1, BL6N1), the Advanced Photon Source (APS) (8ID-D[3], 2ID-D) and SOLEIL (Metrology).

Here, we would like to report the results of the basic evaluation test.

3.1. Experimental setup

Comprehensive basic evaluation was performed at the Metrology beamline[9] at SOLEIL. Depending on the requirement of the test, a configuration using X-ray fluorescence and a configuration using a direct beam were used.

The X-ray fluorescence setup [Fig. 4(a)] was used to evaluate the uniformity and spatial resolution of the detector. A glass plate containing Ge was placed at an angle of 45° to the direct beam axis of a 12 keV beam and placed perpendicular to the detector normal as a secondary target. The 9.9 keV (Ge Kα line) was used.

The direct beam setup [Fig. 4(b)] used a monochromatic direct beam of 9.9 keV to evaluate the response to the input counting rate. The intensity of the beam was adjusted by changing the thickness of the aluminum attenuators. The X-ray beam intensity was monitored by a calibrated photodiode detector placed at the same distance as the XSPA detector.

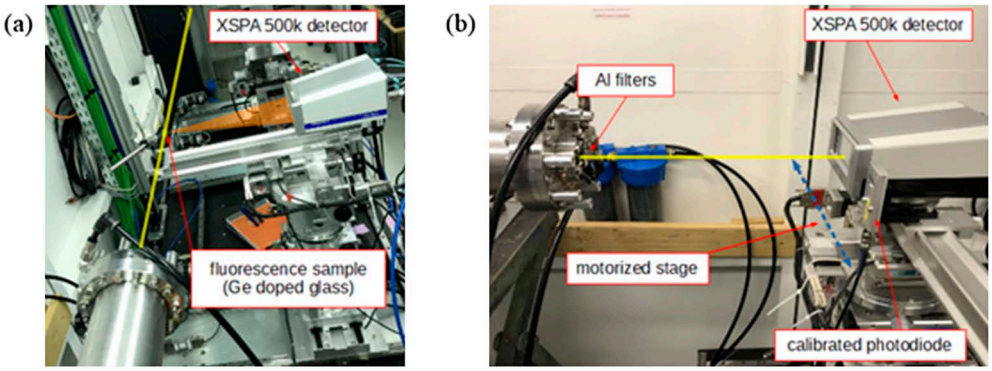

Fig. 4. The experimental setup of the detector in the basic performance evaluation experiment at SOLEIL. On the left is the setup using Ge fluorescence. The Ge sample is placed on the optical path of the direct beam, and the detector is positioned so that it is directly facing the sample. On the right is the setup using a direct beam. The detector is placed in the direct beam path and the Al attenuators are used to tune the beam intensity.

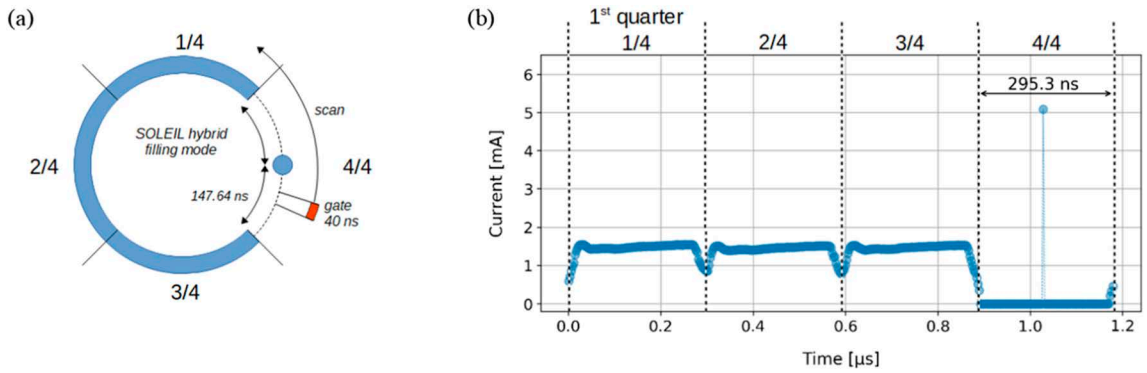

Fig. 5. Schematic diagram of the bunch time structure of the hybrid bunch mode used in this experiment.

During the experiment, the synchrotron was operated in the hybrid bunch mode shown in Fig. 5.

3.2. Experimental results

3.2.1. Uniformity and signal-to-noise ratio

A uniformity correction is applied to the readout value of each pixel to correct the statistical non-uniformity introduced by deviations of the energy threshold value and/or by the sensor. By applying this correction, the Poisson limit of the detector is increased. To obtain a correction coefficient, the detector is irradiated with uniform X-rays of the energy of interest with a sufficient count rate and statistically enough counts for each pixel[10]. A uniformity correction coefficient was obtained using Ge X-ray fluorescence of 9.9 keV irradiated onto the XSPA-500k detector to count approximately 5×10^5 photons/pixel. Two peaks represent the coefficients of the pixel group with two rows of outer circumference, which shows that the outer periphery collects and counts charges in an area wider than the standard pixel size, including the guard ring part. When the uniformity correction coefficient obtained by this method is applied to the uniformly irradiated image of 9.9 keV X-ray, the variation in intensity between the corrected pixels is approximated by a $\sigma = 0.37\%$ normal distribution, and almost all pixels are within the ± 1% range [Fig. 7].

As shown in Fig. 8, the degree to which the signal-to-noise ratio (SNR) increases monotonically with respect to the signal strength is also an important performance indicator of the detector. The Poisson limit of the detector can be directly obtained using the plot[11]. Since the HPC detector is not affected by readout noise, the SNR curve is affected by Poisson noise (shot noise) and fixed pattern noise. The Poisson limit is defined as the reciprocal of the square of the Photon Response Non-Uniformity (PRNU). The PRNU can be obtained by fitting an analytical model to the experimental data, and the Poisson limit has improved by an order of magnitude from about 10^4 photons/pixel/sec to about 10^5 photons/pixel/sec by applying the uniformity correction.

Prior to these analyses, the defective pixels were extracted and masked by comparing the medians with 50×50 peripheral pixels. Pixels that showed less than half or more than twice the intensity of the medians were defined as defective pixels. The number of defective pixels on the XSPA-500k detector was less than 0.02% of the total number of pixels.

3.2.2. Energy resolution

Energy resolution is an essential factor for accurately setting energy thresholds, especially for detectors with multiple thresholds, such as XSPA-500k. It is defined as the full width at half maximum of the peak of the differential curve. The energy resolution was measured for all pixels by scanning the threshold against 9.9 keV Ge Kα fluorescent X-rays. The energy threshold was scanned from 4.0 keV to 18.0 keV in 100 eV increments. An image was measured for each of the energy thresholds, and the average value for the whole module was used. The resulting differential spectrum is shown in Fig. 9 along with the Gaussian fit. The full width at half maximum of the fitted Gaussian function was

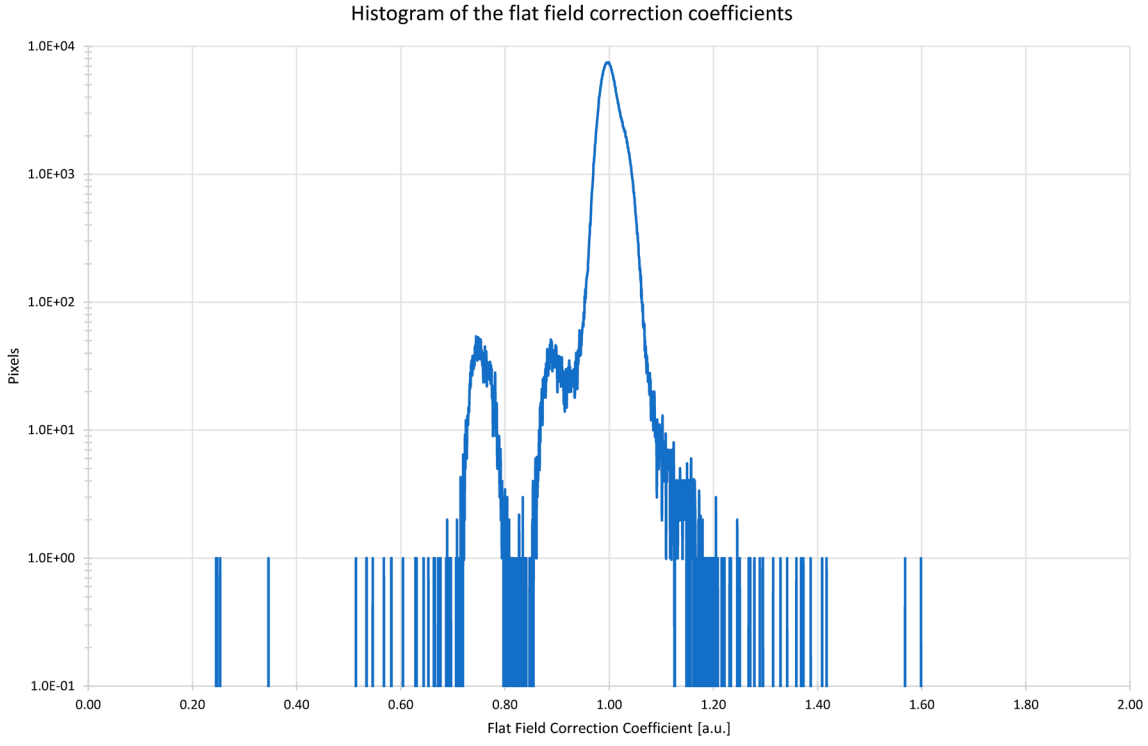

Fig. 6. Distribution of uniformity correction coefficients obtained by uniform irradiation of Ge X-ray fluorescence (9.9 keV). Two small peaks of coefficients in the vicinity of 0.9 and 0.75 can be seen to the left of the main coefficient peak at 1.0.

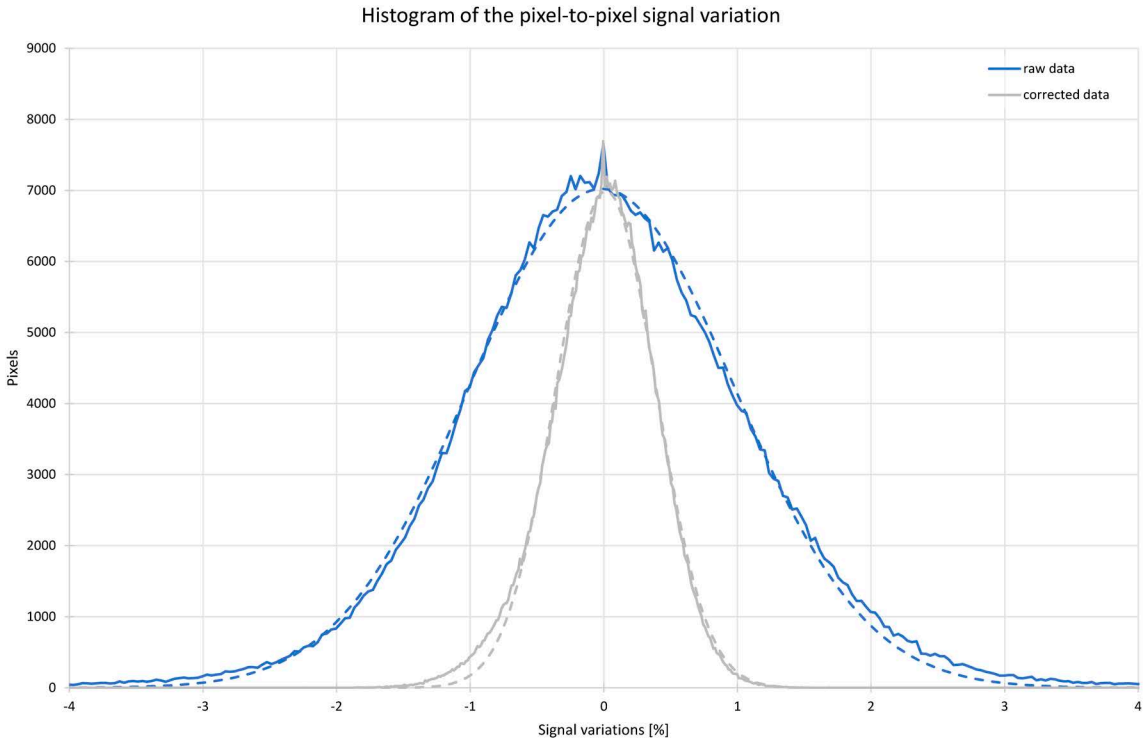

Fig. 7. Variation in intensity for each pixel before and after uniformity correction. Uniformity correction improved the variation from $\sigma = 1.54\%$ to $\sigma = 0.37\%$.

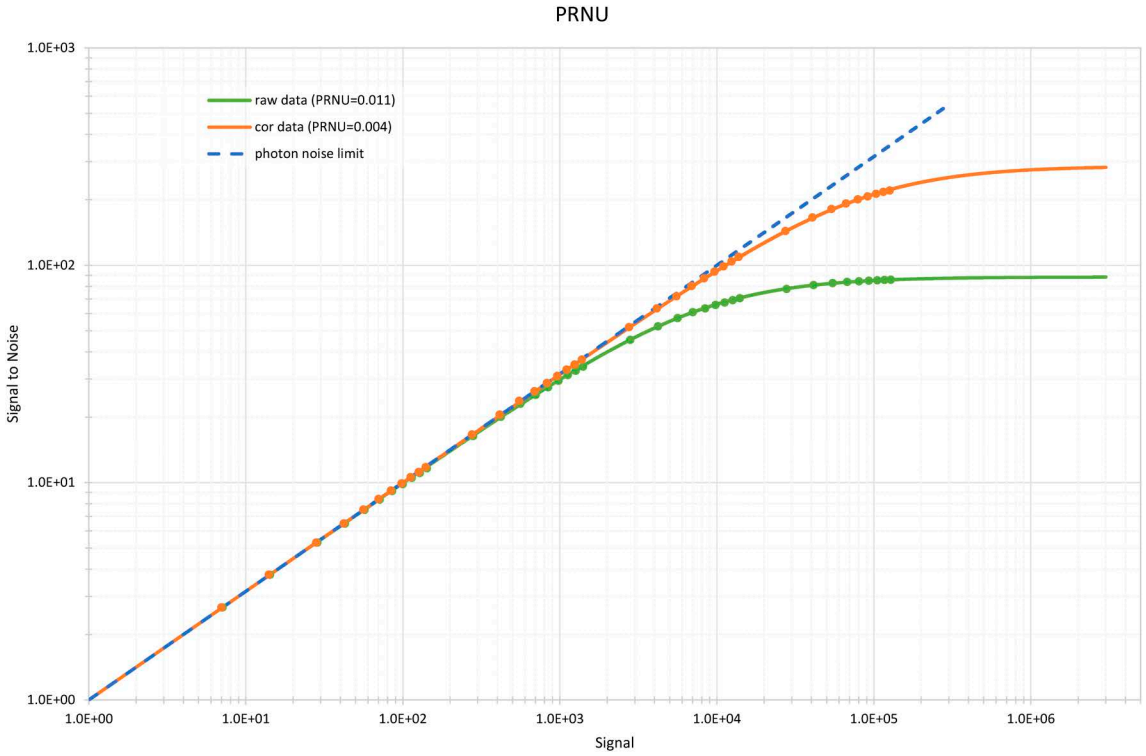

Fig. 8. The signal-to-noise ratio before and after uniformity correction is plotted against the signal intensity. The PRNU has improved by more than an order of magnitude, from 0.11 to 0.0035.

calculated to be 1.5 keV, which is a typical value for a single photon counting pixel detector and is comparable to other state-of-the-art detectors[12].

3.2.3. Count rate linearity

Linearity with respect to the input count rate was measured in a direct beam configuration. As described in Section 2.1, the XSPA detector can change its performance in terms of noise level, energy resolution, and count rate via several settings. During the evaluation test, the "normal" setting was used. This mode uses a very

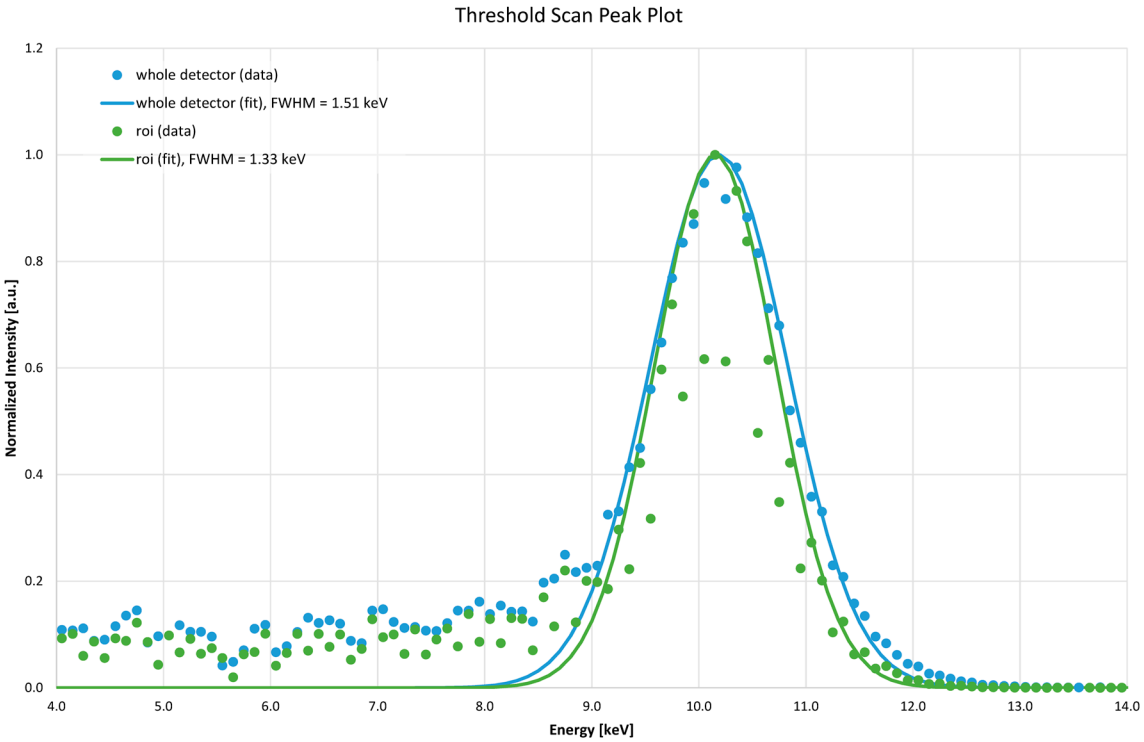

Fig. 9. Differential profile and Gaussian fitting curve of Ge X-ray fluorescence (9.9 keV) obtained by threshold scanning.

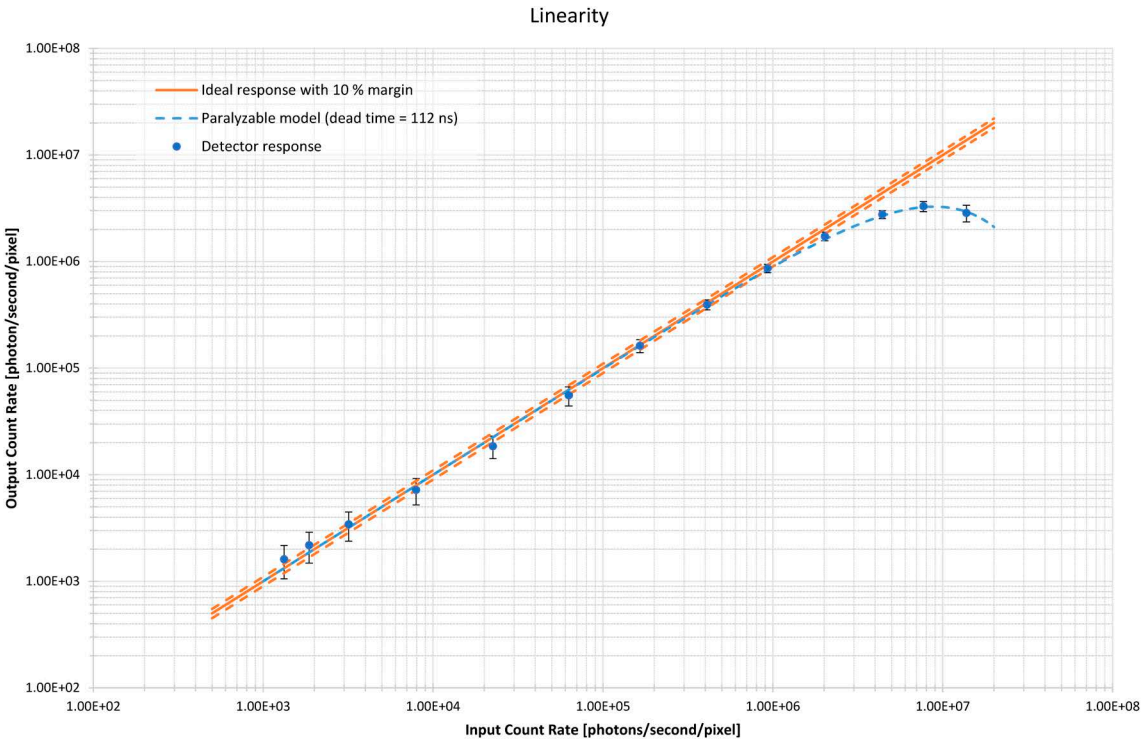

Fig. 10. The measurement result of count rate linearity and the fitting curve by the paralyze model. The counting limit with 10% linearity is about 9.4×10^6 photons/second/pixel from the time constant of 112 ns obtained by fitting.

low feedback current setting in the CSA. (By changing the CSA feedback current, the noise level and pulse width can be changed in a trade-off relationship[8].) Therefore, the result is not a nominal linearity value with DAC settings tuned to achieve the best linearity value, but rather a linearity value measured with practical DAC settings for the real operation of the detector. A direct beam of 9.9 keV was irradiated onto an area of 35×36 pixels. The non-uniformity of the direct beam used at this time was about 7%. The intensity of the beam was

tuned by inserting 125 µm thick aluminum attenuators. The intensity was measured with a calibrated 51 µm thick silicon photodiode for each attenuator thickness to accurately estimate the number of input photons. Both the XSPA detector and the photodiode were placed equidistant from the emission window. The count rate for each pixel was obtained by dividing the total count in the irradiated area by the number of pixels in the area.

The measured data were fitted with the paralyzed model[13] shown below.

N_OUT=N_IN exp(-N_IN tau) where N_OUT is the actual measured output count rate, N_IN is the input count rate, tau is the time constant of the detector. The obtained time constant was 112 ns, and the maximum count rate is 9×10^6 counts/s/pixel (1.6×10^9 counts/s/mm^2).

4. Conclusion

Rigaku and AGH University have developed a detector with high speed and high uniformity. With the cooperation of the SOLEIL detector group, we evaluated the basic performance of the detector at the Metrology beamline. Evaluation of uniformity and signal-to-noise ratio was performed. The intensity variation after uniformity correction can be approximated with a normal distribution of about $\sigma = 0.37\%$, and the Poisson limit is about 10^6 photons/pixel/sec. From the evaluation results of energy resolution and counting rate linearity, the XSPA displays a time constant of 112 ns and a high counting rate linearity of about 10^7 counts/s/pixel, as well as a full width at half maximum of 1.5 keV at 9.9 keV, which is comparable to that of other HPC detectors.

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