Non-destructive characterization of crystallographic defects of SiC substrates using X-ray topography for R&D and quality assurance in production

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1. Introduction

1.1. SiC market overview and application fields

One of the major technical challenges of this decade are energy efficient technologies, which is among others, comparable in its importance to Artificial Intelligence, 5G and IoT. Innovative silicon carbide (SiC) technology and components will contribute significantly towards the goal of a greener, energy efficient and sustainable economy. SiC also addresses major and dynamic growth markets such as renewable energy generation and conversion, edge computing, cloud computing and data centers and last but not least the imminent change to and corresponding growth of electric mobility solutions. SiC is therefore one of the most important semiconducting material in this decade.

Especially power applications require high quality and cost efficient SiC substrates. Currently, one of the main drivers of the overall power market is automotive and will potentially remain the largest one during the next years. SiC is already used in on-board chargers and is expected to be widely used in the coming years. The main inverter market is driving the overall SiC-based electrical vehicle (EV) and hybrid electrical vehicles (HEV) market. An important step for SiC adoption for power electronics happened in 2018 when Tesla decided to adopt this technology for its traction inverter. After two years and almost 1 million cars on the road, SiC demonstrated its ability to support high current and high voltage with very low electrical losses, high thermal and electrical conductivity and reliability. Today most of the leading OEMs are using or will use SiC in their next generation vehicles. 800V battery vehicles represent a significant market opportunity for SiC owing to its interesting performance/cost ratio compared to Si IGBT. Everyone agrees that EV is the market of highest potential, but perceptions differ regarding how it will grow, and how SiC will penetrate the automotive market. Ranging from conservative to optimistic, players from the industry offer very different forecasts in terms of market value for SiC in the EV and HEV market. Market analyses converge to say that SiC semiconductor market will explode in the coming years reaching a total device revenue of more than 5 Billion $ in 2025. This revenue corresponds roughly to 1.8 Billion pieces of devices produced in 2025 on an equivalent of more than 3 Million 150 mm SiC wafers. Yole[1, 2] expects the SiC EV/HEV market, from SiC substrate up to device and module, to grow from $225M in 2019 to beyond $1.5B in 2025. This trend is clearly visible also in the electrification level of vehicles[3]. Furthermore, an overall growth for the SiC power device market from $500M in 2019 to more than $2.5B in 2025 is expected [1].

Beyond automotive, the next big drivers for the SiC power market is photovoltaic (PV) inverters and EV/HEV charging infrastructure, compare Figure 1. The photovoltaic (PV) market is growing fast. To bring down costs of the installation, one of the main requirements is to increase the efficiency of the PV inverters. Hybrid SiC modules are deployed in >30 kW systems and full SiC modules are penetrating the >100 kW string inverters actually. EV/HEV charging infrastructures, especially high power charges (<200 kW), are in the focus for integrating SiC-based devices. These show clear benefits compared to Si-based devices. These main three application fields, automotive, PV and charging infrastructure covered already 65% of the overall SiC power market in 2019 and will potentially cover more than 80% in 2025.

At the SiC wafer level, the total addressable market follows the same exponential trend as shown in Figure 1 and is expected to grow by a factor of more than 10 within the next 5 years. In this context and based on major players forecasts, the gap between the worldwide SiC bulk capacity and the demand is expected to grow

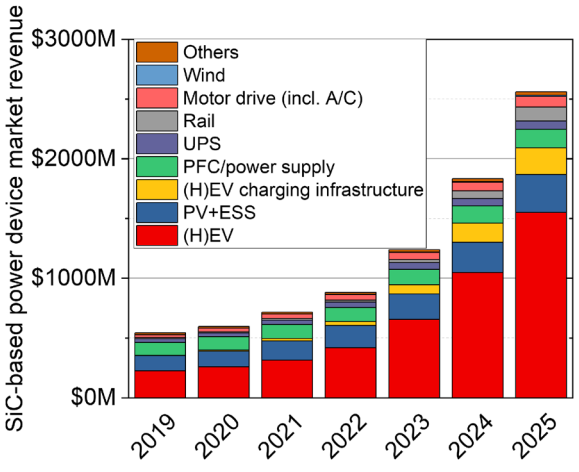

Fig. 1. Projected development of the SiC power device market reported by Yole [1] in 2020.

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in the coming years and reach 500 k Wafers by 2023 and more than 2 Million 150 mm Wafers in 2027. This expected imbalance between supply and demand is a first barrier to SiC adoption and brings the focus on the SiC material sources worldwide. Due to the current undersupply of SiC substrates, the obtained prices for typical 150 mm n-type SiC wafers are quite high and in the range of $800–$1200 per wafer, depending on the material quality and the purchased quantity. Beside wafer prices, the material quality is a very important factor to choose the right material supplier. A stable baseline, instead of handpicking small numbers of best case wafers, for supplying high quality SiC substrates is needed to manufacture reliable SiC power devices, which is especially requested for automotive application. Therefore, a strong need for non-destructive and reliable SiC substrate characterization occurs, which supports R&D purposes, e.g. defect optimization or scale up to 200 mm substrate diameter, and of course in-line capability in terms of quality assurance within production environment.

1.2. Center of Expertise for X-ray Topography at Fraunhofer IISB

This said, Rigaku Corporation Japan, Rigaku Europe SE and Fraunhofer IISB in Erlangen, are pleased to announce the formation of the Center of Expertise for X-ray Topography worldwide, located in Erlangen, Germany. The purpose of this cooperation is to support the semiconductor industry worldwide, e.g. in the area of SiC, in improving and better understanding their wafer quality and yield by employing the Rigaku XRTmicron advanced X-ray topography tools. One focus is to find operation procedures, tailored to the specific needs of different customers. Further, together we develop measurement routines and quantification algorithms suitable for the requirements of the industry, particularly the request for a high throughput in the production environment.

Founded in 1985, the Fraunhofer Institute for Integrated Systems and Device Technology IISB conducts applied research and development in the fields of power electronics, energy electronics, and semiconductors on the foundation of the Fraunhofer model. As a result, the institute comprehensively covers the value-added chain for complex electronics systems, from the basic material to complete electronics and energy systems. Research focuses on the application areas of electromobility and energy supply. For its customers, the institute develops solutions in the fields of material development, semiconductor technology and manufacturing, electronic components, devices and modules, construction packaging and connection technology, simulation, reliability, up to system development in vehicle electronics, energy electronics, and energy infrastructure. Among other things, the IISB has extensive know-how in semiconductor basic material and characterization. A unique factor at Fraunhofer IISB is the fully integrated SiC value chain, from SiC homoepitaxy, to the power device as well as module and system integration.

2. SiC Substrate Quality Challenges and Device Yield Limitations

SiC boules are produced by the Physical Vapor Transport (PVT) method, in which SiC powder is sublimated and transported as Si_2C, Si and SiC_2 from the high temperature sublimation area at the crucible bottom to the lower temperature top part were a SiC seed is placed and the crystal can grow [5]. Subsequently, the SiC boules are separated from the top and bottom part to achieve a usable length, which is typically in the range of 20 to 50 mm depending on the growth process and material supplier. To achieve the final substrate diameter (100, 150 or 200 mm), the boules are cylindrically grinded. The resulting so-called pucks are then separated into single substrates with a typical thickness of 350 μm using multiwire saws or specially designed splitting processes[6]. A final epi ready surface finish is applied mandatory to the side intended for the subsequent homo-epitaxial growth, which usually is the Si-face of the wafer.

The quality of the SiC bulk substrate is mainly determined by the presence and density of remaining structural defects, such as micropipes (MP), threading edge (TED), threading screw (TSD), threading mixed (TMD) and basal plane dislocations (BPD), as well as stacking faults (Shockley type (SSF) and Frank type (FSF)) and locally concentrated SiC polytype phases. For most of these defects, it is highly challenging to detect them and determine their density on SiC substrate material because standard routines such as KOH etching and photoluminescence imaging only work with strong restrictions due to the high doping level. The structural defects in the substrate are also often the origin of epitaxial defects. Figure 2 shows potential defect propagation scenarios depending on the defect type occurring typically in the SiC substrate. While TEDs,

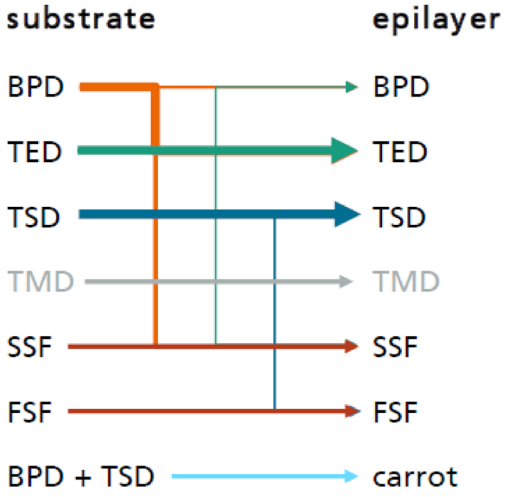

Fig. 2. Potential defect propagation scenarios depending on the defect type occurring already at the SiC substrate based on [4].

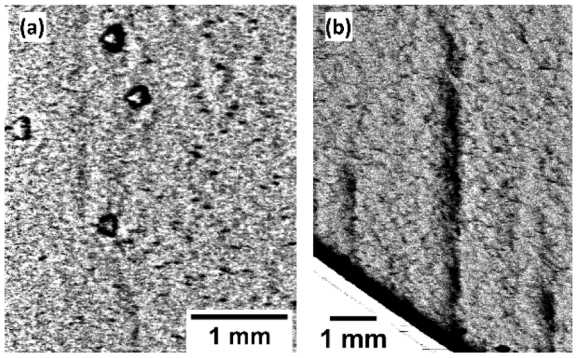

Fig. 3. Example of different stacking faults in epi layers, left: triangle-shaped stacking fault observed in the topogram of the (008)-reflex, right: bar-shaped stacking faults observed in the (118)-reflex. The flat points down in both images.

TSDs, TMDs and FSFs penetrate from the substrate through the SiC epilayer, growth conditions are typically chosen such that over 90% of the BPDs are converted into TEDs. Remaining BPDs can lead to SSFs in the epilayer and in combination with TSD, BPDs can also lead to the so called carrot defect.

It is well known that in-grown stacking faults, i.e. SSFs and FSFs, and carrots or triangular morphological defects, are the main yield-limiting defects for power devices[6]. An example of such crystal defect is shown in Figure 3. For instance, the triangular SSFs or bar-shaped stacking faults can grow in the final device during bipolar field operation of e.g. the internal body diode of a SiC MOSFET. Depending on the amount of defects, the static device losses may increase significantly over time, e.g. due to the increase of the drain-source on resistance RDS(on). Therefore, the root cause of such defects like basal-plane dislocations, initially present in the substrate, must be reduced as much as possible.

3. X-ray Topography for R&D and Quality Assurance in Production Environment

Due to the tremendously increasing SiC wafer production capacity over the next years, wafer inspection and metrology will become more critical in the SiC industry. Especially substrate and power device manufacturers need to have a deep understanding about the substrate quality in terms of crystallographic defects, their distribution along the whole wafer area and the absolute quantities. Therefore, Rigaku introduced a new X-ray topography system (XRTmicron) already in 2013[8], which gives the possibility to investigate different crystallographic defects in SiC substrates with high resolution on full wafer scale. In the framework of the Center of Expertise for X-ray topography, Fraunhofer IISB has developed new measurement routines and defect quantification algorithms which can fulfil the industrial needs in terms of throughput, reliability and accuracy.

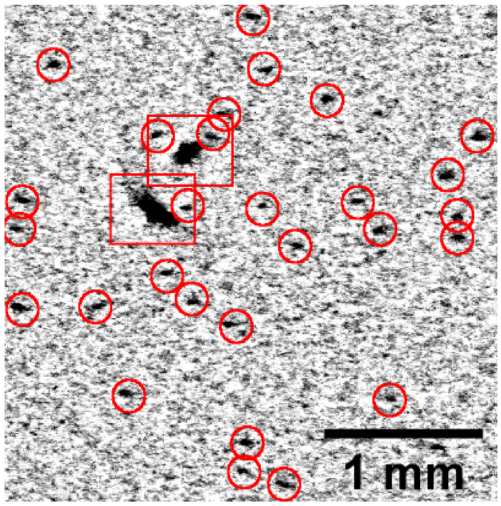

Fig. 4. X-ray topogram showing TSDs (circles, exemplary) and two micropipes (rectangles)

3.1. TSD detection

Using Rigaku's lab-scale XRTmicron tool we started quantifying the TSD density on full wafer scale. Screw dislocations have been one of the most urgent issue in the industry because a TSD detection based on KOH etching is at least complicated[9], which is why usually TSD densities are not part of wafer specification list, even though they may have a strong impact on the device performance[10]. In an X-ray topogram, these defects can be easily recognized and distinguished from other defects as they appear as strongly contrasted, oval spots with approximate dimensions of $50\,\mu m \times 30\,\mu m$ (see Figure 4) in the topogram of the (008) reflex of Cu Kα radiation. We developed a detection and counting algorithm, allowing an automated determination of the defect density within a processing time of less than 5 minutes for a full 150 mm wafer on a decent desktop PC. The accuracy of this algorithm comes very close to a manual counting as can be seen by a comparison between the dark spots and red marks in Figure 5. We further verified that the spots appearing in the topograms are indeed related to TSDs. For that purpose, we investigated surface pits forming at every position of the TSD in an epitaxial layer applied on top of the substrate. These were detected by differential interference contrast microscopy and their position is highlighted in yellow in Figure 5. A comparison to KOH etching of the epi layers not shown here yielded a similar, almost perfect agreement. Based on this approach, it is possible to obtain a TSD density map on full wafer scale in less than two hours—a time scale unimaginable to be realized at a synchrotron. Two sample TSD mappings are exemplarily displayed in Figure 6.

For industrial purposes, slight compromises regarding completeness of information and accuracy can often be made for the sake of a further increased throughput. To speed up measurements, the XRTmicron allows investigating only fractions of the wafer area. Next to the full wafer mapping (A), two such possibilities (B

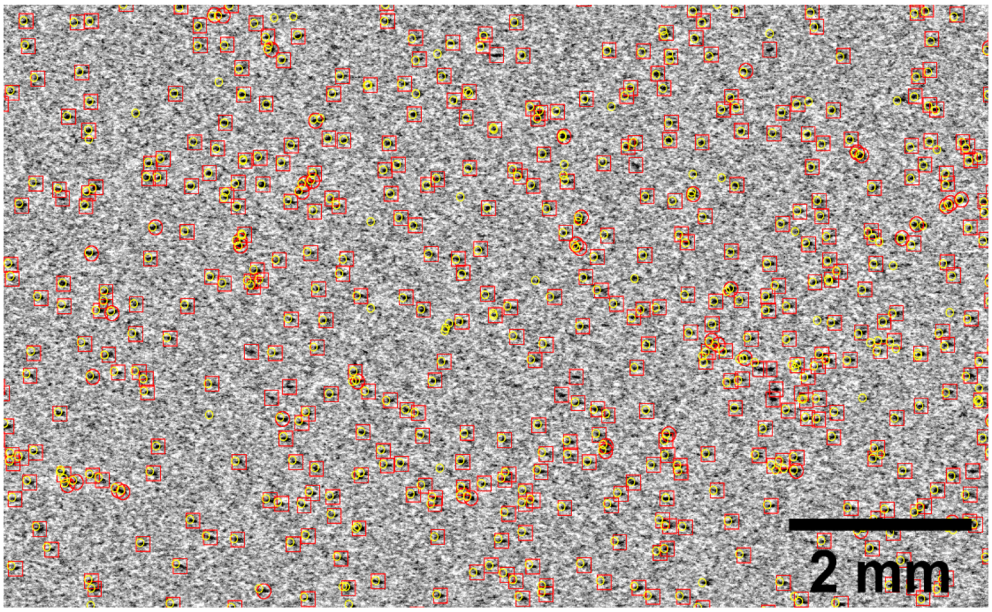

Fig. 5. X-ray topogam of a 4H-SiC wafer with epi layer, overlayed with TSDs detected by XRT (red rectangles) and pits detected by Differantial Interference Contrast (DIC) microscopy (yellow circles) showing a very good agreement between both approaches.

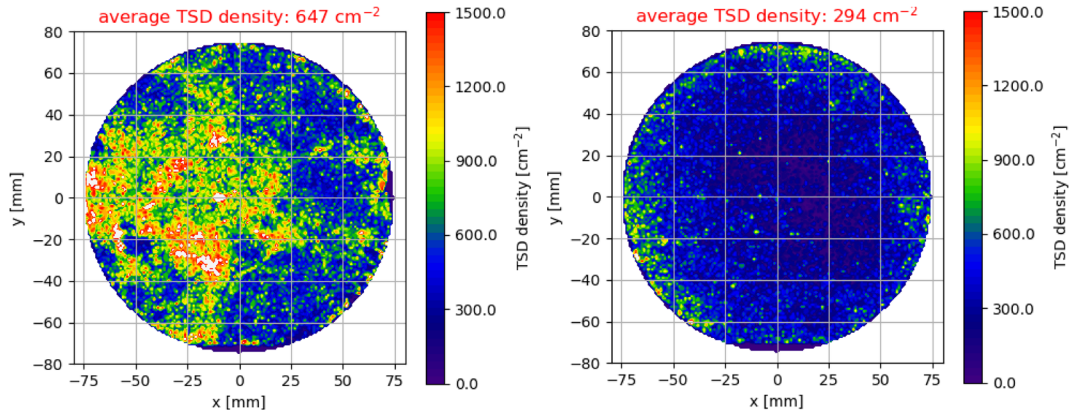

Fig. 6. Full-wafer TSD density maps of a wafer with higher TSD density (left) and one with lower TSD density (right).

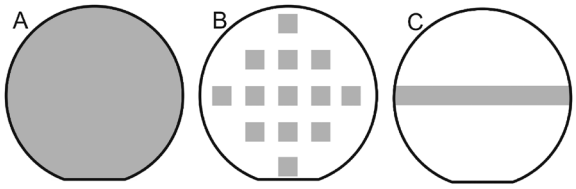

Fig. 7. Illustration of the measurement plans, regions to be analyzed are highlighted in grey.

and C) are shown in Figure 7. The grid of squares (B) is an established approach in the semiconductor industry and regularly used e.g. for etch pit counting. Since the image height covered by the CCD covers a length of up to 16.5 mm on the wafer, an edge size of the squares up to this value gives the greatest benefit in measurement time. A reasonable option for such a measurement plan is then to use squares with 15 mm edge length and 15 mm spacing in between, resulting in 13 fields to be measured on a 150 mm wafer.

Similarly, the most natural way to reduce measurement time based on the measurement principle of the XRT is the measurement of a stripe through the diameter (C) with the same preferences regarding stripe height. While a full wafer mapping without measurement time optimizations takes about 2 hours including alignment and evaluation, a throughput of 2 wafers/h can be achieved using the grid measurement and almost 3 wafers/h are possible for the stripe measurements.

In order to understand the error of these only local measurements to determine the average defect density of the full wafer, we evaluated the TSD density for several wafers based on all three approaches. Taking the results for the full wafer as reference, we found root mean square deviations of 4.9% for the grid

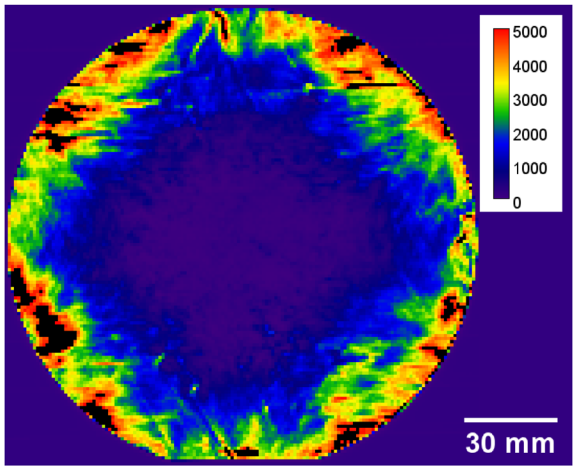

Fig. 8. BPD density map generated based on XRT measurements. The scale gives the BPD density per cm^2.

measurement and 16.5% for the stripe measurement if calculating the average TSD density on the measured area without weighting. The largest errors found were 11.7% for the grid measurement and 36.9% for the stripe measurement, both for a strongly inhomogeneous wafer. Typically, the error resulting from the grid measurement is considered to be fully acceptable. In contrast, the error found for the stripe measurement approach is problematic. However, this error mainly results from an overrepresentation of the wafer center in the measured area. By taking this issue into account and thus applying a radial weighting of the TSD density, the deviation relative to the full wafer analysis can be reduced down to a root mean square of 6.6% and a maximum observed value of 12.9%. Using this approach, the added uncertainty is well in line with the differences in measurement time, opening a wide range of options to choose from.

3.2 Other defects

Also for other types of defects, we are currently jointly developing analysis algorithms and measurement routines. For example, the detection of micropipes is more or less a side product of TSD analysis. In addition, our approach to determine the BPD density is far advanced. The challenge here is that industry requires the values to be consistent to EPD results because of comparability to established routines and, more importantly, because only BPDs intersecting with the growth interface will affect the quality of the epi layer. In this on-going work, we already could bring down the measurement time for a full wafer map to 1 h (including alignment) with probably further potential for improvement. The results we obtain were calibrated against established BPD measurements based etch pit counting after KOH etching and show a very good correlation to these data. An example is shown in Figure 8.

The detection of stacking faults and TEDs is also highly relevant for the assessment of the wafer quality and are also in development.

4. Summary

In this contribution, we demonstrate the application of Rigaku's lab-scale XRT technique to quantify the threading-screw dislocation (TSD) and basal plane dislocation (BPD) density on full wafer scale designed for industrial needs. Our results clearly show that defect quantification in SiC bare wafers reaches a higher level by using a lab-scale XRT system, which brings substantial benefits for R&D and quality assurance issues in production along the SiC value chain.

References

(1) Yole Développement: "*Power SiC: Materials, Devices and Applications 2020 - Market and Technology Report 2020*".

(2) Yole Développement: "*Compound Semiconductor Quarterly Market Monitor, Q3 2020*".

(3) Yole Développement: "*Power Electronics for e-Mobility 2021 - Market and Technology Report 2021*".

(4) T. Kimoto and J. A. Cooper (Eds): "*Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*", Wiley-IEEE, 2014.

(5) P. J. Wellmann: *Semicond. Sci. Technol.*, **33** (2018), 103001.

(6) M. Swoboda, R. Rieske, C. Beyer, A. Ullrich, G. Gesell and J. Richter: *Materials Science Forum*, **963** (2019), 10–13.

(7) T. Kimoto, A. Iijima, H. Tsuchida, T. Miyazawa, T. Tawara, A. Otsuki, T. Kato and Y. Yonezawa: *In 2017 IEEE International Reliability Physics Symposium (IRPS)*, (2017), 2A–1.1–2A–1.7.

(8) K. Omote: *The Rigaku Journal*, **29** (2013), No. 1, 1–8.

(9) B. Kallinger, S. Polster, P. Berwian, J. Friedrich, G. Müller, A. N. Danilewsky, A. Wehrhahn and A.-D. Weber: *J. Cryst. Growth*, **314** (2011), 21–29.

(10) T. Kimoto and J. A. Cooper (Eds): "Effects of Extended Defects on SiC Device Performance" in "*Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*", *Wiley-IEEE*, 2014, pp. 161–165.